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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,264	03/10/2004	Matthias H. Regelsberger	H10210/JDP	5357

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EXAMINER	
PHAM, HAI CHI	

ART UNIT	PAPER NUMBER
2861	

MAIL DATE	DELIVERY MODE
02/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/797,264	REGELSBERGER ET AL.	
	Examiner	Art Unit	
	Hai C. Pham	2861	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 21 January 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,6,26-29,32-36 and 39*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Hai C Pham/
Primary Examiner, Art Unit 2861
02/05/08

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's arguments filed 01/21/07 are not persuasive.

First of all, the examiner respectfully disagrees with the overall estimate of Sawada's method steps 1-8 advanced by the Applicant in his remarks. The following is the estimate of Sawada's method steps 1-8 as construed by the examiner, re-using Applicant's own statement and steps:

1. Step S11: applying an initial drive current to the respective LEDs in the single chip or subset under consideration, i.e. LED chip 10-1;

2. Step S12: measuring the light-emission quantity of each LED of that single chip;

3. Step S13: temporarily allotting the time correction value to every LED of that single chip based on the measured light-emission quantity of each LED to make the light-emission quantity of the respective LEDs uniform, the time correction value being not the same for every LED in that single chip;

4. Step S14: calculating the exposure energy of the respective LEDs of that single chip based on the temporary time correction value of the applied drive current;

5. Step S15: calculating the "average exposure energy EA of a chip" (last two sentences of [0019]) based on the exposure energy of the respective LEDs of that single chip;

6. Step 16: comparing the average exposure energy EA of that single chip with a predetermined desired value E0, the desired value E0 being the "final average exposure energy of all chips built into a print head" (see [0024]);

7. Step S17: altering the applied drive current for the respective LEDs of the single chip based on the comparison result obtained in step 6 (S16), and if the average exposure energy EA of that single chip is not the same as the predetermined desired value E0, repeating steps 2-6 until the average exposure energy EA of that single chip is the same as the predetermined desired value E0; and

8. operating the respective LEDs of that single chip using the altered drive current.

Sawada further teaches that the above method steps being performed separately for every chip (see [0024]).

In accordance with the teaching of Sawada, claim 1 is rejected as follows:

- calculating a light-output correction for each of a plurality of subsets of the LEDs (the LEDs 12 are organized into a plurality of LED chips 10-1 through 10-3), each subset being controlled by a respective one of a plurality of different controllers (each of the plural LED chips 10-1 to 10-3 is driven by a corresponding drive circuit 14-1 to 14-3) (Fig. 3), each light-output correction for one of the LED subsets being calculated based at least upon factors pertaining to

(a) a light output from the one LED subset associated with the light-output correction being calculated for that subset (the emission quantity is measured for each LED in the chip and the emission quantity correction adjusts the light intensity of each LED in that chip based on the measured emission quantity), and

(b) an average light output from the plurality of subsets of the LEDs (the average exposure energy EA of a chip is calculated based on the exposure energy of the respective LEDs of that single chip and is compared to the predetermined desired value E0, which is the "final average exposure energy of all chips built into a print head") (see [0019], [0024]); wherein each light-output correction for one of the LED subsets, facilitates correction of the light output from its associated LED subset as function of applied voltage or supplied current (the adjustment of the emission of the LEDs in the chip is made by altering the time duration applied to the supplied current from the corresponding drive circuit, and the adjustment is performed separately for every chip) ([0024]); and

- adjusting the light output from the LED subsets as a function of applied voltage or supplied current in accordance with their corresponding light-output corrections (the emission quantity of the LED in each chip is adjusted based on the correction values obtained separately for each chip) ([0024]),

- wherein each of the plurality of subsets of the LEDs includes more than one LED (each LED chip 10 has a plurality of LEDs 12-1 to 12-64).

Finally, in response to Applicant's argument that "in Sawada any light-output correction that the Examiner construes to be disclosed in Sawada would [be] a single light-output correction for all the LED subsets," the examiner would like to direct Applicant's attention to the disclosure of Sawada at paragraph [0024], which clearly indicates that the adjustment of the emission quantity of the LEDs in the chip is performed "separately for every chip". In other words, the light-output correction value varies form one chip to another